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IEEE STD. IEEE Standard

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1. Improved multicast switch architecture for optical cable television and video surveillance networks

 Kariniemi, H.; Nurmi, J.;
 Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on
 Volume 4, 23-26 May 2004 Page(s):IV - 221-4 Vol.4

[AbstractPlus](#) | Full Text: [PDF](#)(282 KB) IEEE CNF


2. An MCM-D module using newly structured thermal management technique

 Yamanaka, N.; Harada, A.; Kaizu, K.; Kawamura, T.;
 IEMT/IMC Symposium, 2nd 1998
 15-17 April 1998 Page(s):255 - 260
 Digital Object Identifier 10.1109/IEMTIM.1998.704632

[AbstractPlus](#) | Full Text: [PDF](#)(544 KB) IEEE CNF

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<u>L1</u>	"field programmable gate array" or FPGA	21036	<u>L1</u>

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<u>L5</u>	710/305,100,316,300;326/37-39;365/185.01,185.11;711/104;716/16.ccls.	8203	<u>L5</u>
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<u>L2</u>	L1 near10 ("static random access memory" or SRAM)	1029	<u>L2</u>
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Default operator:

12 and (programmable adj1 connector)

	U	I	Document ID	Issue Dat	Pages	Title	Current OR	Current X
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6897679	20050524	46	Programmable logic	326/41	326/38
			B2			array integrated circuit		
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6799240	20040928		SRAM bus architecture	710/305	710/100;
			B1			and interconnect to an		716/16
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6759870	20040706		Programmable logic	326/41	326/38
			B2			array integrated circuit		
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6417690	20020709		Floor plan for scalable	326/41	712/37;
			B1			multiple level tab orie		712/38
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6404225	20020611		Integrated circuit	326/39	326/37;
			B1			incorporating a program		326/41
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6362646	20020326		Method and apparatus	326/40	326/41;
			B1			for reducing memory res		326/47
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6326807	20011204		Programmable logic	326/40	326/38;
			B1			architecture incorporat		326/39;
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6300793	20011009		Scalable multiple level	326/41	326/47
			B1			tab oriented interconne		
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6292017	20010918		Programmable logic	326/40	326/38;
			B1			device incorporating fu		365/230.0
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6249143	20010619		Programmable logic	326/40	326/39
			B1			array integrated circuit		
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6195788	20010227		Mapping heterogeneous	716/18	716/16